WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

(a) a wiring substrate having a first surface and a second surface opposing said first surface, first pads being formed over a first region of said first surface, while second pads being formed over a second region surrounding said first region;

(b) a microcomputer chip having bump electrodes formed over a surface thereof, said microcomputer chip being mounted over said first region of said wiring substrate such that said first pads and said bump electrodes are electrically connected to each other; and

(c) a memory chip having third pads formed over a surface thereof, said memory chip being mounted over a back surface of said microcomputer chip, said third pads being connected to said second pads by use of conductive wires.

2. A semiconductor device according to claim 1, wherein the number of said bump electrodes is larger than that of said third pads.

3. A semiconductor device according to claim 1, wherein said wiring substrate is a build-up substrate.

4. A semiconductor device according to claim 1, wherein a minimum pitch of said first pads or of said second pads is 65 μm or less.

5. A semiconductor device comprising:

(a) a wiring substrate having a first surface and a second surface opposing said first surface, first pads being formed over a first region of said first surface, while second pads being formed over a second region surrounding said first region;

(b) a microcomputer chip having bump electrodes formed over a surface thereof, said microcomputer chip being mounted over said first region of said wiring substrate such that said first pads and said bump electrodes are electrically connected to each other; and

(c) first and second memory chips mounted over a back surface of said microcomputer chip,

(c1) said first memory chip having third pads formed over a surface thereof,

(c2) said second memory chip having fourth pads formed over a surface thereof,

(c3) said third and second pads being connected to said second pads by use of conductive wires.

6. A semiconductor device according to claim 5, wherein the number of said bump electrodes is larger than a sum of the respective numbers of said third and fourth pads.

7. A semiconductor device according to claim 5, wherein said wiring substrate is a build-up substrate.

8. A semiconductor device according to claim 5, wherein a shortest pitch of said first pads or of said second pads is

65 μm or less.

9. A semiconductor device according to claim 5, wherein each of said first and second memory chips is controlled by said microcomputer chip.

10. A semiconductor device according to claim 5, wherein

(d) wherein a width of said microcomputer chip in a first direction is smaller than a sum of respective widths of said first and second memory chips in said first direction,

wherein said microcomputer chip has a pair of edges extending in a second direction orthogonal to said first direction,

wherein said first memory chip protrudes outwardly from one of said pair of edges, and

wherein said second memory chip protrudes outwardly from the other of said pair of edges.

11. A semiconductor device according to claim 5, wherein each of said first and second memory chips protrudes by a distance of 1.5 mm or less from the corresponding one of said pair of edges of the microcomputer chip.

12. A semiconductor device according to claim 5, wherein each of said first and second memory chips protrudes by a distance of 1 mm or less from the corresponding one of said pair of edges of edges of the microcomputer chip.

13. A semiconductor device according to claim 5,

wherein each of said first and second memory chips is thinner than said microcomputer chip.

14. A semiconductor device according to claim 5, wherein each of said first and second memory chips has a thickness of 200 μm or less.

15. A semiconductor device according to claim 5, wherein a resin is filled in a space under a portion of each of said first and second memory chips protruding from said pair of edges of said microcomputer chip.

16. A semiconductor device according to claim 5, wherein each of said first and second memory chips is a DRAM or a nonvolatile memory.

17. A semiconductor device according to claim 5, wherein said third and fourth pads are arranged in linear configurations at respective center portions of the memory chips or arranged in linear configurations along respective two opposing edges of the memory chips.

18. A semiconductor device according to claim 17, wherein said first and second chips have said third and fourth pads arranged along edges of said microcomputer chip and connected to said second pads by use of said conductive wires such that they do not extend over the other memory chip.

19. A semiconductor device according to claim 5, wherein said third pads are connected to said second pads by use of said conductive wires such that do not extend over

said second memory chip and said fourth pads are connected to said second pads by use of said conductive wires such that they do not extend over said first memory chip.

20. A semiconductor device comprising:

(a) a wiring substrate having a first surface and a second surface opposing said first surface, first pads being formed over a first region of said first surface, while second pads being formed over a second region surrounding said first region;

(b) a microcomputer chip having bump electrodes formed over a surface thereof, said microcomputer chip being mounted over said first region of said wiring substrate such that said first pads and said bump electrodes are electrically connected to each other; and

(c) a plurality of memory chips mounted over a back surface of said microcomputer chip, each of the memory chips having third pads formed over a surface thereof, said third pads being connected to said second pads by use of conductive wires.